CLAIMS

1. A method for operating one or more transistors, comprising:

providing a transistor comprising a buried channel layer intermediate to a source and a drain, and a surface layer intermediate to the buried layer and a gate;

applying a voltage to the gate to control a current between the source and the drain; and

causing the current to flow predominately through the buried channel layer by applying a back-bias voltage to the transistor to modulate a free charge carrier density distribution in the buried layer and in the surface layer.

2. The method of claim 1, wherein applying the back-bias voltage comprises substantially preventing formation of an inversion region in the surface layer.

3. The method of claim 1, wherein applying the back-bias voltage comprises selecting the back-bias voltage in cooperation with the gate voltage to cause radio frequency operation of the transistor.

4. The method of claim 1, wherein applying the voltage to the gate comprises selecting a range of gate voltages to operate the transistor in a substantially linear drain current versus source voltage condition.

5. The method of claim 1, wherein applying the voltage to the gate comprises operating the transistor as an analog device.

6. The method of claim 5, wherein operating the transistor comprises operating the transistor as a power device.

7. The method of claim 1, wherein the buried channel layer has a heterojunction interface.

8. The method of claim 1, wherein the buried channel layer comprises a strained semiconductor.

9. The method of claim 8, wherein the surface layer comprises a semiconductor that is substantially strain-free.

10. The method of claim 8, wherein the buried layer is intermediate to the surface layer and a relaxed layer comprising silicon and germanium.

11. The method of claim 8, wherein the strained semiconductor is under tensile strain, and applying the back-bias voltage comprises causing the buried channel layer to provide an n-type channel, and further comprising providing a second transistor associated with the first transistor and comprising a second buried channel layer comprising a semiconductor under compressive strain, and further comprising applying a second back-bias voltage to the second transistor to cause the second buried channel layer to provide a p-type channel.

12. The method of claim 1, wherein the buried channel layer comprises a quantum well.

13. The method of claim 1, wherein applying the back-bias voltage comprises applying the back-bias voltage to one of a substrate and an intermediate layer adjacent to the transistor.

14. A semiconductor device, comprising:

a transistor comprising a buried channel layer intermediate to a source and a drain, and a surface layer intermediate to the buried layer and a gate;

a terminal facilitating application of a voltage to the gate to control a current between the source and the drain; and

a charge carrier modulator facilitating application of a back-bias voltage to the transistor to modulate a free charge carrier density distribution in the buried layer and in the surface layer to cause the current to flow predominately through the buried channel layer.

15. The device of claim 14, wherein the buried channel layer comprises a semiconductor under tensile strain.

16. The device of claim 15, wherein the buried channel layer consists substantially of silicon.

17. The device of claim 15, wherein the buried channel layer comprises silicon and germanium.

18. The device of claim 14, wherein the buried channel layer has a heterojunction interface that is associated with a heterojunction offset, the offset promoting confinement of free charge carriers in the buried channel layer.

19. The device of claim 18, wherein the heterojunction offset is one of a type I offset and a type II offset.

20. The device of claim 18, wherein the buried channel layer is a quantum well.

21. The device of claim 14, wherein the device is an analog device.

22. The device of claim 14, wherein the buried channel layer comprises a semiconductor under compressive strain.

23. The device of claim 22, wherein the buried channel layer consists substantially of germanium.

24. The device of claim 22, wherein the buried channel layer comprises silicon and germanium.

25. The device of claim 14, further comprising a relaxed layer comprising silicon and germanium, in contact with the buried layer on a side opposite to the surface layer.

26. The device of claim 14, wherein the buried channel layer comprises a semiconductor under tensile strain providing an n-type channel, and further comprising a second transistor associated with the first transistor and comprising a second buried channel layer comprising a second semiconductor under compressive strain providing a p-type channel.